

DATA SHEET



MPEG) (Multichannel

SAA2505H **DUET digital multichannel audio IC**

Preliminary specification
Supersedes data of 1998 Mar 10
File under Integrated Circuits, IC01

2001 Apr 05

DUET digital multichannel audio IC

SAA2505H

FEATURES

Hardware features

- Two 40 MIPS 20-bit DSP cores
- All input and output buffer RAM is on-chip
- Program ROM on-chip for all decoding modes
- Two I²S-bus inputs with normal, double and quad speed mode (slave only)
- Second serial input usable for ADC (Karaoke input)
- Three normal and double speed I²S-bus outputs (slave and master from 256 and 384f_s)
- One normal, double, quad speed I²S-bus output (slave and master from 256 and 384f_s)
- Japanese EIAJ serial input and output formats
- Sony Philips Digital Interface (SPDIF) output
- I²C-bus control (up to 400 kHz)
- 3.3 V supply with 5 V TTL compatible inputs/outputs
- Boundary scan for printed-circuit board testing.

Software features

- AC-3 up to 5.1 channels
- MPEG 2 L2 up to 7.1 channels
- MPEG 1 L2 (Video-CD) 2 channels at 44.1 kHz
- Dolby pro-logic decoding at 32, 44.1 and 48 kHz
- Output configuration for 7, 5, 4, 3, 2 and 1 channels with or without Low Frequency Enhancement (LFE)
- Bass redirection for small satellite loudspeakers plus subwoofer
- Karaoke voice mix
- Dynamic range compression (AC-3 and MPEG)
- Adjustable delay up to 15 ms for surround channels (1.5 kbyte words)
- Adjustable delay up to 5 ms for centre channel (250 words)
- Rounding to DAC word length
- Mute by pin and I²C-bus command
- AC-3 and MPEG bitstream information available via the I²C-bus
- Concealment of CRC errors
- SPDIF coded output
- Fully programmable SPDIF channel status information.



APPLICATIONS

The SAA2505H is intended for all markets where a multi-channel audio decoder for Dolby AC-3 and MPEG 2 is required.

Primary markets are for DVD video players, TV sets and audio/video amplifiers.

GENERAL

The SAA2505H decodes multi-channel audio up to MPEG 7.1, AC-3 5.1 and pro-logic on a dual DSP core.

The device contains all of the RAM and ROM necessary for operation. This minimises the need for external components and no microcode download is required.

The device is primarily intended for audio/video surround sound amplifiers where the amplifier is connected to the data source by means of SPDIF (IEC 60958). The input interface is, therefore, made for SPDIF (IEC 60958) and formatted for the I²S-bus.

The primary device output is PCM, sent via four I²S-bus ports. There is also a SPDIF (IEC 60958) formatted output.

User control is achieved via an I²C-bus. However, the SAA2505H is capable of stand-alone operation.

DUET digital multichannel audio IC

SAA2505H

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DDD}	digital supply voltage		3.0	3.3	3.6	V
I _{DDD}	digital supply current		–	160	–	mA
V _{DDA}	analog supply voltage		3.0	3.3	3.6	V
I _{DDA}	analog supply current		–	tbf	–	mA
f _{xtal}	crystal frequency		–	35	–	MHz
T _{amb}	operating ambient temperature		0	–	70	°C
V _{ESD}	electrostatic discharge sensitivity for all pins	note 1	–2000	–	+2000	V
		note 2	–300	–	+300	V

Notes

- Human body model: equivalent to discharging a 100 pF capacitor through a 1500 Ω resistor.
- Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω resistor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2505H	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

DUET digital multichannel audio IC

SAA2505H

BLOCK DIAGRAM

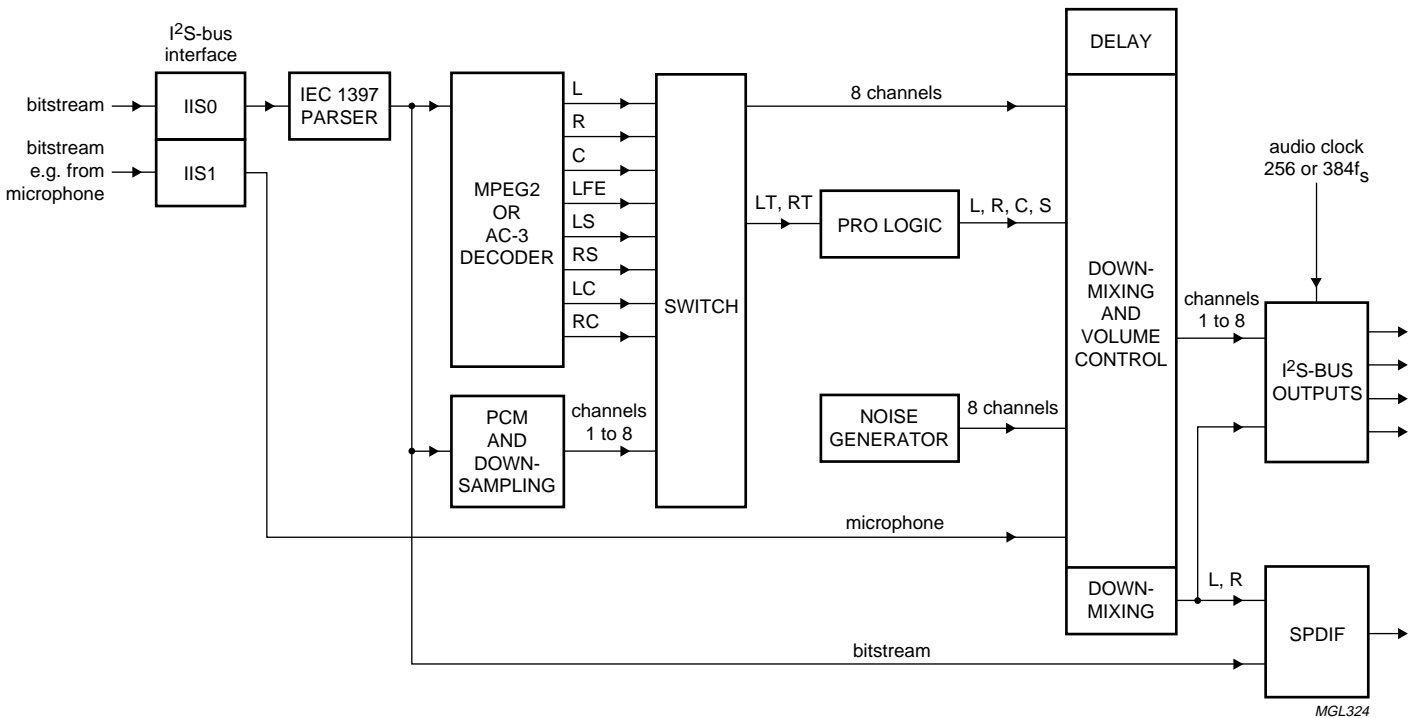


Fig.1 Simplified block diagram.

DUET digital multichannel audio IC

SAA2505H

PINNING

SYMBOL	PIN	DRIVE/ LOAD ⁽¹⁾	TYPE	DESCRIPTION
STANDALONE	1	A	I	select stand-alone mode input
EFO1	2	F	O	output flag FO1; from DSP2
EFO2	3	F	O	output flag FO2; from DSP2
EFO3	4	F	O	output flag FO3; from DSP2
EFO4	5	F	O	output flag FO4; from DSP1
EFO5	6	F	O	output flag FO5; from DSP1
EFO6	7	F	O	output flag FO6; from DSP1
V _{SSDI}	8	–	S	digital ground for internal logic and memories; note 2
V _{DDDI}	9	–	S	digital supply voltage for internal logic and memories (+3.3 V); note 3
EFI1	10	A	I	input flag FI1; to DSP2
EFI2	11	A	I	input flag FI2; to DSP1
EFI3	12	A	I	input flag FI3; to DSP1
V _{DDDE}	13	–	S	digital supply voltage for I/O cells (+3.3 V); note 4
WSO	14	G	I/O	word select input/output for ports 0 to 2; also used for output port 3 when not in quad mode (I ² S-bus)
SCK	15	G	I/O	serial clock input/output for ports 0 to 2; also used for output port 3 when not in quad mode (I ² S-bus)
V _{SSDE}	16	–	S	digital ground for I/O cells; note 5
SDO0	17	F	O	serial data output for port 0 (I ² S-bus)
SDO1	18	F	O	serial data output for port 1 (I ² S-bus)
V _{DDDE}	19	–	S	digital supply voltage for I/O cells (+3.3 V); note 4
V _{SSDI}	20	–	S	digital ground for internal logic and memories; note 2
V _{DDDI}	21	–	S	digital supply voltage for internal logic and memories (+3.3 V); note 3
V _{SSDI}	22	–	S	digital ground for internal logic and memories; note 2
V _{DDDI}	23	–	S	digital supply voltage for internal logic and memories (+3.3 V); note 3
V _{DDDI}	24	–	S	digital supply voltage for internal logic and memories (+3.3 V); note 3
V _{SSDI}	25	–	S	digital ground for internal logic and memories; note 2
V _{DDDE}	26	–	S	digital supply voltage for I/O cells (+3.3 V); note 4
SDO2	27	F	O	serial data output for port 2 (I ² S-bus)
SDO3	28	F	O	serial data output for port 3 (I ² S-bus)
V _{SSDE}	29	–	S	digital ground for I/O cells; note 5
WSO3	30	F	O	word select output for port 3; used in quad mode (I ² S-bus)
SCKO3	31	F	O	serial clock output for port 3; used in quad mode (I ² S-bus)
V _{DDDE}	32	–	S	digital supply voltage for I/O cells (+3.3 V); note 4
SDB	33	F	O	serial data begin output for port 3; used in quad mode (I ² S-bus)
SPDIF	34	F	O	SPDIF output
V _{SSDE}	35	–	S	digital ground for I/O cells; note 5
V _{SSDI}	36	–	S	digital ground for internal logic and memories; note 2
V _{DDDI}	37	–	S	digital supply voltage for internal logic and memories (+3.3 V); note 3

DUET digital multichannel audio IC

SAA2505H

SYMBOL	PIN	DRIVE/ LOAD ⁽¹⁾	TYPE	DESCRIPTION
V _{SSDE}	38	–	S	digital ground for I/O cells; note 5
SYSCLK	39	E	O	programmable system clock output
V _{DDDE}	40	–	S	digital supply voltage for I/O cells (+3.3 V); note 4
V _{DDA}	41	–	S	analog supply voltage for crystal oscillator (+3.3 V)
CLKI	42	H	I	oscillator input
CLKO	43	H	O	oscillator output
V _{SSDA}	44	–	S	digital ground for crystal oscillator
ACLK	45	A	I	audio clock input for master mode
V _{SSDE}	46	–	S	digital ground for I/O cells; note 5
TDI	47	B	I	boundary scan test data input (this pin should be pulled HIGH for normal operation)
TMS	48	B	I	boundary scan test mode select input (this pin should be pulled HIGH for normal operation)
TCK	49	B	I	boundary scan test clock input
$\overline{\text{TRST}}$	50	B	I	boundary scan test reset input (this pin should be pulled LOW for normal operation)
TDO	51	B	O	boundary scan test data output
V _{DDDI}	52	–	S	digital supply voltage for internal logic and memories (+3.3 V); note 3
V _{SSDI}	53	–	S	digital ground for internal logic and memories; note 2
WSI	54	A	I	word select input for ports 0 and 1 (I ² S-bus)
SDBI	55	A	I	serial data begin input for port 0 (I ² S-bus)
SDI0	56	A	I	serial data input for port 0 (I ² S-bus)
SDI1	57	A	I	serial data input for port 1 (I ² S-bus)
SCKI	58	A	I	serial clock input for ports 0 and 1 (I ² S-bus)
V _{SSDI}	59	–	S	digital ground for internal logic and memories; note 2
V _{DDDI}	60	–	S	digital supply voltage for internal logic and memories (+3.3 V); note 3
RESET	61	C	I	hardware reset
ADDR	62	A	I	select address input (I ² C-bus)
SCL	63	C	I	serial clock input; external pull-up to +5 V (I ² C-bus)
SDA	64	D	I/O	serial data input/output; external pull-up to +5 V (I ² C-bus)

Notes

1. See Table 1.
2. All V_{SSDI} pins are internally connected.
3. All V_{DDDI} pins are internally connected.
4. All V_{DDDE} pins are internally connected.
5. All V_{SSDE} pins are internally connected.

DUET digital multichannel audio IC

SAA2505H

Table 1 Pin drive and load descriptions

DRIVE/LOAD	DESCRIPTION
A	+5 V tolerant input; TTL characterized with internal pull-down resistor
B	+5 V tolerant input; TTL characterized with internal pull-up resistor
C	+5 V tolerant input; TTL Schmitt-trigger characterized
D	+5 V tolerant 400 kHz (I ² C-bus)
E	TTL characterised +5 V tolerant 3-state output with 3 mA drive capability
F	TTL characterised +5 V tolerant 3-state slew rate limited output with 3 mA drive capability
G	+5 V tolerant bidirectional 3-state pin; with 3 mA output drive and slew rate limiting; TTL level input; without pull-up or pull-down resistor
H	crystal pins

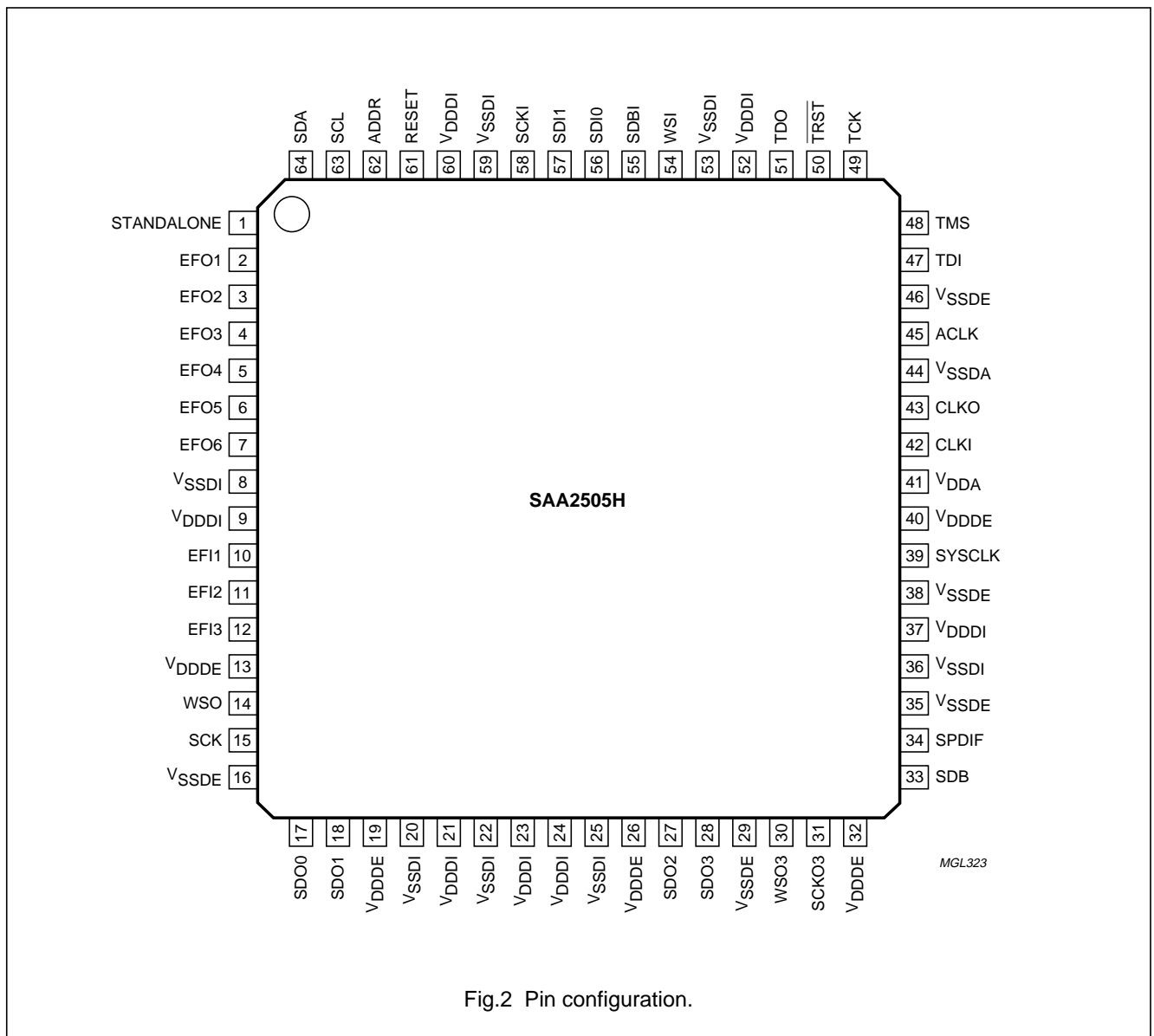


Fig.2 Pin configuration.

DUET digital multichannel audio IC

SAA2505H

CLOCK BUILD-UP

Up to four clocks provide the timing information for the SAA2505H. These are as follows:

1. Data source clock
2. Data processing clock
3. I²C-bus data/control clock
4. Data sink clock.

Data source clock

Clocking of the input data is derived from the serial clock input at pin 58 and is compliant with the I²S-bus and EIAJ transfer formats. The ports are capable of operating at normal, double and quad speed.

Data processing clock

This clock is used for data processing and internal data transfer. The clock can either be provided by an external clock generator having a duty cycle between 40 and 60% or by using the internal crystal clock generator and an external crystal. The external clock should be connected between pins 42 (CLKI) and 43 (CLKO) (see Fig.11).

To use the internal clock a 35 MHz crystal operating on the 3rd harmonic must be connected between pins 42 and 43 (CLKI and CLKO).

A buffered version of this clock is available at pin 39 (SYSCLK). This can be optionally disabled or, a divided version (4, 2 and 1) of the clock input at pin 42 (CLKI) can be made available.

I²C-bus data/control clock

The I²C-bus control logic supports I²C-bus clock speeds up to 400 kHz. This is supplied to pin 63 (SCL). If the SAA2505H is in the stand-alone mode (pin 1 HIGH) no I²C-bus clock needs to be supplied.

Data sink clock

The data sink clock source is dependant on the mode of operation of the I²S-bus output ports.

In the master mode the I²S-bus clock is derived from an external 256 or 384f_s source connected to pin 45 (ACLK). This is internally divided and used to drive the serial clock at pins 15 and 31 (SCK and SCKO3). To ensure that the digital outputs poses good timing qualities (jitter and wander) pin 45 should be a connected to a high quality timing source.

In the I²S-bus slave mode the output data is clocked to pin 15. This can either be the serial clock input at pin 58 (SCKI) or a suitable external clock. When in slave mode the signal at pin 15 is replicated at pin 31.

FUNCTIONAL DESCRIPTION**Data sinks**

Coded audio data or PCM audio data can be input to both DSPs from two slave-only serial interfaces capable of receiving data in either I²S-bus or EIAJ formats. Both serial interfaces use the same serial clock (pin 58) and word select input (pin 54). The serial clock must be at least 32f_s.

Serial data is applied to pins 56 and 57 (SDI0 and SDI1). These pins are mode shared between the I²S-bus and EIAJ formatted serial data. Port mode selection is achieved via the I²C-bus interface, see Table 3.

I²S-BUS FORMATTED SPDIF INFORMATION

In the I²S-bus mode 'big-endian' data is received, MSB justified to 1 clock period after a falling edge of the word select output. The data stream should be formatted according to "IEC 60958 - SPDIF" including the extensions for non-PCM encoded audio data ("IEC 61937").

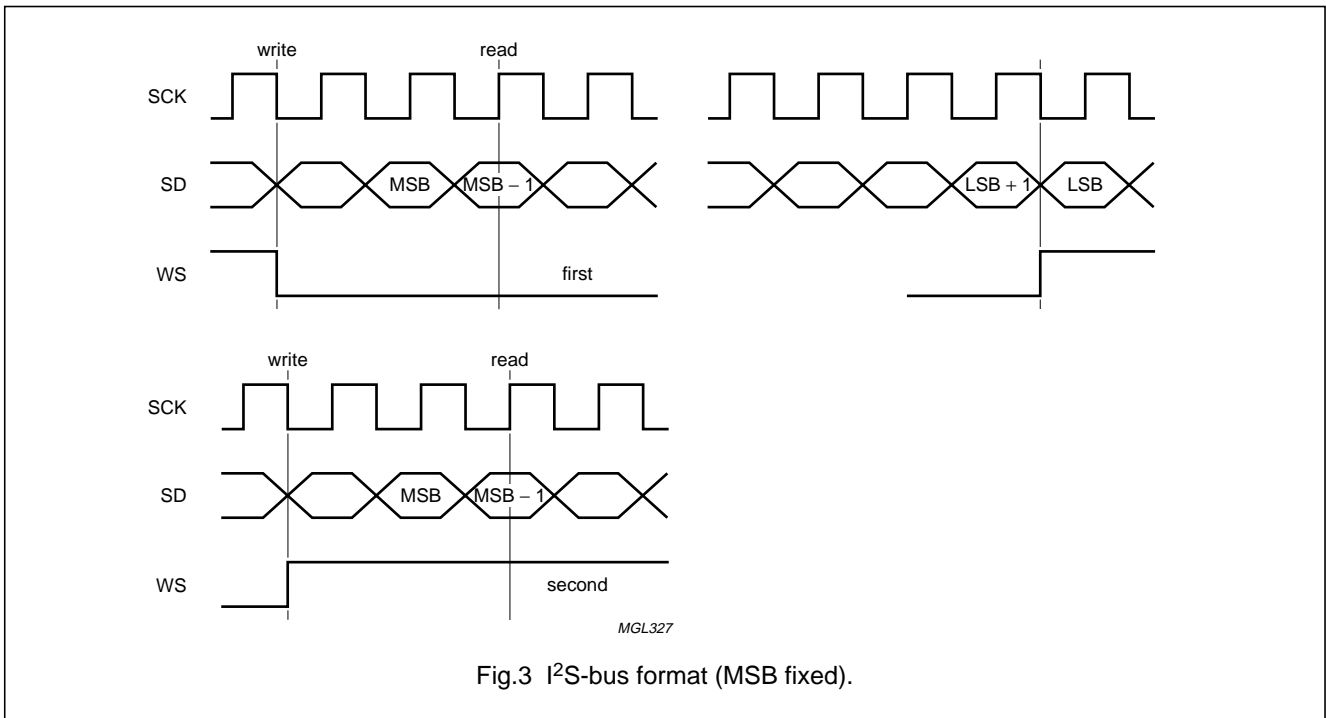
AC-3 and MPEG coded data is formatted in 16-bit words. These words are expected at a sample rate (f_s) of 48 kHz and thus a minimum serial clock of 1.536 MHz; two 16-bit words per word select period. If the transmission word length is in excess of 16 bits all additional bits are discarded.

PCM sample lengths of up to 20-bit words are supported with sample rates of 44.1 and 48 kHz. This mode is used to transfer PCM and PCM with Dolby pro-logic encoded data. Word select LOW corresponds to transmission of data for the left channel, word select HIGH corresponds to transmission of data for the right channel.

Pin 55 (SDBI) is reserved for a multi-channel extension to the I²S-bus and is currently not supported.

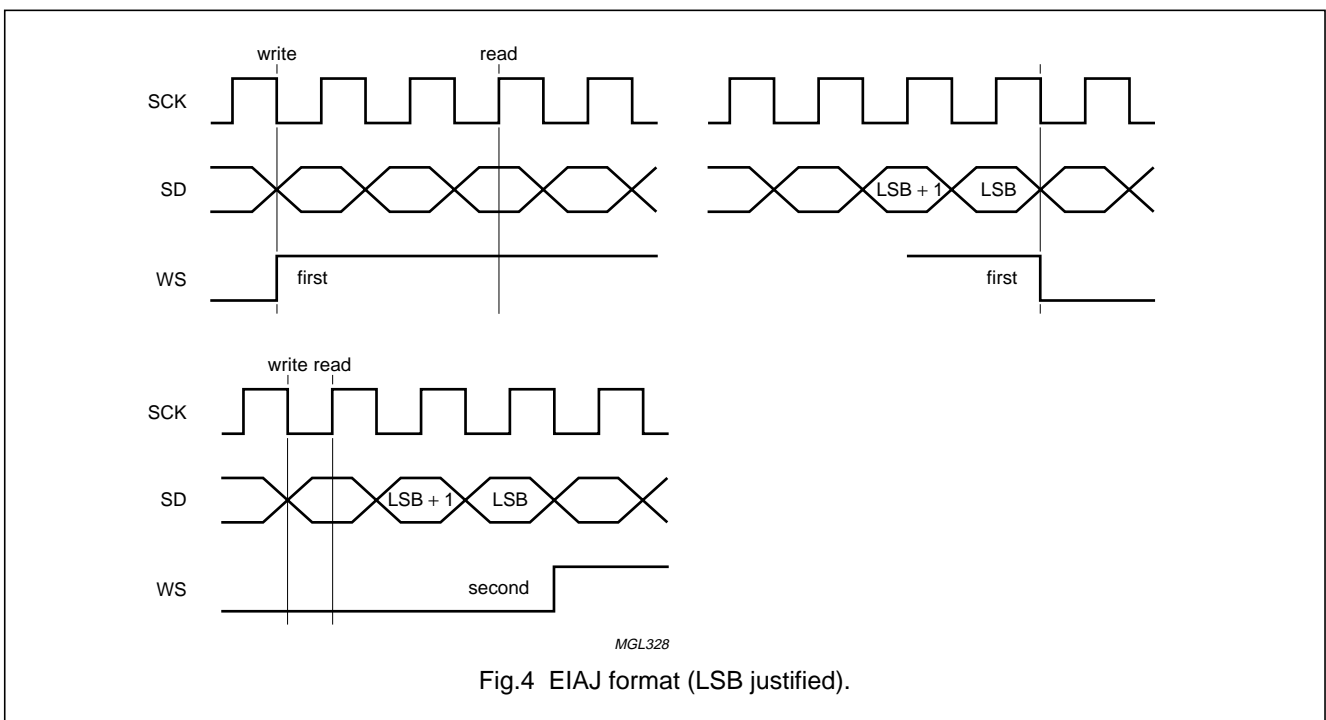
DUET digital multichannel audio IC

SAA2505H



EIAJ FORMATTED INPUTS

In EIAJ mode 'big-endian' data is received LSB justified to the rising edge of word select output. Formatting of the data is identical to that used in the I²S-bus mode.



DUET digital multichannel audio IC

SAA2505H

Data sources**I²S-BUS AND EIAJ FORMATTED OUTPUTS**

The device has four I²S-bus/EIAJ mode select outputs. These outputs are capable of outputting data in EIAJ 20, 18 or 16-bit and I²S-bus modes. The EIAJ outputs are capable of operating in single or double speed, the I²S-bus output is capable of operating in single, double and quad speed.

The output ports can either be in the slave or master mode. In the slave mode they can either be slaved to the I²S-bus serial clock input (pin 15) or to an external clock. In the master mode an audio clock is applied to pin 45 that is 256 or 384f_s. The master clocking scheme allows the support of a 96 kHz sample rate DAC by use of the double speed output option. The quad speed output option is intended to allow multiple SAA2505H devices to be connected together.

In order to obtain a high quality digital output in the master mode the audio clock should be of high quality, having low jitter and an even mark space ration.

SPDIF FORMATTED OUTPUT

The SPDIF output can transmit either coded data, as received from the serial data input at pin 56 (SDI0), or down-mixed 20-bit PCM stereo. The down-mixed stereo may be Pro-logic encoded.

Together with the PCM samples additional control bits are transmitted. These are the channel status, user data and validity bits.

The first five bytes of the channel status bits are user programmable, all following bytes are zeroed automatically. Transmission is LSB first.

The user data can carry message lengths of 129 bytes. These are transmitted over the SPDIF port at a rate of 2 bits per stereo sample. The message buffer of 129 bytes is loaded via the I²C-bus, if no message is written the SAA2505H outputs all zeros for the user data.

Table 2 Output port timing information

MODE	AUDIO CLOCK SAMPLING FREQUENCY	WORD SELECT SAMPLING FREQUENCY	SERIAL CLOCK SAMPLING FREQUENCY	SERIAL DATA BEGIN SAMPLING FREQUENCY
Single	256 or 384f _s	1f _s	64f _s	–
Double	256 or 384f _s	2f _s	128f _s	–
Quad	256f _s	4f _s	256f _s	1f _s
Quad	384f _s	4f _s	192f _s	1f _s

Control Inputs

The SAA2505H can be operated in two stand-alone modes or can be managed by the I²C-bus.

STAND-ALONE MODES

Two stand-alone modes exist to allow the device to be used in systems without a microcontroller. These two modes are STANDALONE (pin 1) held HIGH and STANDALONE connected to RESET (pin 61).

When pin 1 is LOW a reset defaults the outputs to quiet, however when pin 1 is HIGH a reset defaults the I²S-bus output to active and the SPDIF output to mute. When pin 1 is HIGH some of the I²C-bus registers cannot be accessed see Table 3.

I²C-BUS REGISTER CONTROL

The I²C-bus port supports 5 V, 400 kHz operation. The details of the registers are given in Table 3.

DUET digital multichannel audio IC

SAA2505H

Table 3 I²C-bus control register

SECTION	REGISTER NAME	MEMORY ADDRESS	DEFAULT VALUE			DESCRIPTION
			1 ⁽¹⁾	2 ⁽²⁾	3 ⁽³⁾	
General	SOFT_RESET	\$8 000-b0	0	0	0	0: operation
						1: reset
General	SYSCLKEN	\$8 000-b1	0	note 4	1	0: enable SYSCLK output
						1: disable SYSCLK output
General	SYSCLKDIV	\$8 000-b3 and b2	00	note 4	10	00: SYSCLK = ¼CLK
						01: SYSCLK = ½CLK
						10: SYSCLK = CLK
						11: reserved
General	EN_INP_INT_DSP1	\$8 000-b4	0	note 4	1	0: disable input interrupts on DSP1
						1: enable input interrupts on DSP1
General	EN_OUTP_INT_DSP1	\$8 000-b5	0	note 4	0	0: disable output interrupts on DSP1
						1: enable output interrupts on DSP1
General	EN_INP_INT_DSP2	\$8 000-b6	0	note 4	1	0: disable input interrupts on DSP2
						1: enable input interrupts on DSP2
General	EN_OUTP_INT_DSP2	\$8 000-b7	0	note 4	0	0: disable output interrupts on DSP2
						1: enable output interrupts on DSP2
General	ACLKSEL	\$8 000-b8	0	note 4	0	0: ACLK = 256f _s
						1: ACLK = 384f _s
General	MEMCONFIG	\$8 000-b9	0	note 4	0	0: program memory on DSP1 = 12 kbytes
						0: program memory on DSP2 = 8 kbytes
						1: program memory on DSP1 = 8 kbytes
						1: program memory on DSP2 = 12 kbytes
I ² SCONTROL	IISMODE	\$8 001-b1 and b0	00	note 4	00	00: I ² S-bus/EIAJ input format
						01: reserved
						10: reserved
						11: reserved
I ² SCONTROL	IISINP	\$8 001-b2	0	note 4	0	0: I ² S-bus input format
						1: EIAJ 16-bit input format
I ² SCONTROL	IISI_SDB_EN	\$8 001-b3	0	note 4	0	0: SDBI is DSP1 Input flag
						1: SDBI is aligned to WS to allow multi-channel I ² S-bus input

DUET digital multichannel audio IC

SAA2505H

SECTION	REGISTER NAME	MEMORY ADDRESS	DEFAULT VALUE			DESCRIPTION
			1 ⁽¹⁾	2 ⁽²⁾	3 ⁽³⁾	
I ² SCONTROL	reserved	\$8 001-b4	0	note 4	0	reserved
I ² SCONTROL	IISOUTMOD	\$8 001-b6 and b5	00	note 4	00	00: I ² S-bus format data output
						01: EIAJ 16-bit format data output
						10: EIAJ 18-bit format data output
						11: EIAJ 20-bit format data output
I ² SCONTROL	IISOUTMST	\$8 001-b7	0	note 4	0	0: I ² S-bus outputs are slaves
						1: I ² S-bus outputs are masters
I ² SCONTROL	IISOUTSPD	\$8 001-b8	0	note 4	0	0: I ² S-bus outputs 0 to 2 operate at normal speed
						1: I ² S-bus outputs 0 to 2 operate at double speed
I ² SCONTROL	IIS3OUTSPD	\$8 001-b10 and b9	00	note 4	00	00: I ² S-bus output 3 operates at normal speed
						01: I ² S-bus output 3 operates at double speed
						10: I ² S-bus output 3 operates at quad speed
						11: I ² S-bus output 3 operates at normal speed
I ² SCONTROL	IISO0EN	\$8 001-b11	0	note 4	1	0: SDO0 output 3-stated
						1: SDO0 output enabled
I ² SCONTROL	IISO1EN	\$8 001-b12	0	note 4	1	0: SDO1 output 3-stated
						1: SDO1 output enabled
I ² SCONTROL	IISO2EN	\$8 001-b13	0	note 4	1	0: SDO2 output 3-stated
						1: SDO2 output enabled
I ² SCONTROL	IISO3EN	\$8 001-b14	0	note 4	1	0: SDO3 output 3-stated
						1: SDO3 output enabled
I ² SCONTROL	IIS3CLKEN	\$8 001-b15	0	note 4	0	0: SCKO3, WSO3 and SDB outputs 3-stated
						1: SCKO3, WSO3 and SDB outputs enabled
SPDIF1	SPDIFVAL	\$8 002-b0	0	0	0	0: SPDIF validity bit = 0
						1: SPDIF transmitting valid PCM
SPDIF1	SPDIFBYP	\$8 002-b1	0	0	0	0: output PCM data from DSP1
						1: output I ² S-bus data from I ² S-bus input
SPDIF1	IISUBIT	\$8 002-b2	0	0	0	reserved
SPDIF1	SPDIFEN	\$8 002-b3	0	0	0	0: 3-state SPDIF output and reset SPDIF block
						1: enable SPDIF output

DUET digital multichannel audio IC

SAA2505H

SECTION	REGISTER NAME	MEMORY ADDRESS	DEFAULT VALUE			DESCRIPTION
			1 ⁽¹⁾	2 ⁽²⁾	3 ⁽³⁾	
Normal usage						
SPDIF1	CSBYTE0	\$8 002-b15 to b8	0000	0000	b8: consumer mode	
					b9: LPCM	
					b10: copy protection	
					b11 to b13: pre-emphasis	
					b14 to b15: mode	
SPDIF2	CSBYTE1	\$8 003-b7 to b0	0000	0000	b0 to b7: category code	
SPDIF2	CSBYTE2	\$8 003-b15 to b8	0000	0000	b8 to b11: source	
					b12 to b15: channel number	
SPDIF3	CSBYTE3	\$8 003-b7 to b0	0000	0000	b0 to b3: source	
					b4 to b6: clock accuracy	
SPDIF3	CSBYTE4	\$8 003-b15 to b8	0000	0000	b0 to b3: word length	

Notes

1. STANDALONE held LOW.
2. STANDALONE held HIGH.
3. STANDALONE connected to RESET.
4. Controlled by DSP; no I²C-bus access.

All unused bits return a value of 0.

DUET digital multichannel audio IC

SAA2505H

I²C-bus control and commands (pins 63 and 64)

INTRODUCTION

A general description of "*The I²C-bus and how to use it*" can be obtained from Philips sales offices using ordering number 9398 393 40011.

For the external control of the SAA2505H a fast I²C-bus is implemented. This is a 400 kHz bus which is downward compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP program; programming the coefficient RAM and reading the values of parameters
- Instructions controlling source selection and programmable parts; through the control registers as detailed in Table 3.

The detailed description of the I²C-bus and commands is given in the following sections.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are the serial data line (SDA) and the serial clock line (SCL). Both lines must be connected to the supply rail via a pull-up resistor when connected to the output stages of a microcontroller. For a 400 kHz I²C-bus, the recommendation from Philips Semiconductors must be followed (e.g. up to loads of 200 pF on the bus a pull-up resistor can be used, between 200 and 400 pF a current source or switched resistor must be used). Data transfer can only be initiated when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 400 kHz. To be able to run at this high frequency all of the Inputs and outputs connected to the bus must be designed for this high speed I²C-bus according the Philips specification (see Fig.5).

START AND STOP CONDITIONS

Both data and clock line will remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as a STOP condition (P) (see Fig.6).

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a START condition (S) (see Fig.6).

DATA TRANSFER

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.7).

ACKNOWLEDGE

The number of data bits transferred between the START and STOP conditions from the transmitter to the receiver is not limited. Each byte of 8 bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level left on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull-down the SDA line, left HIGH by the transmitter, during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must be taken into account. A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition (see Fig.8).

STATE OF THE I²C-BUS INTERFACE DURING AND AFTER POWER-ON RESET

During power-on reset the internal SDA line is kept HIGH and the SDA pin is therefore high impedance. The SDA line remains HIGH until a master pulls it down to initiate communication.

DUET digital multichannel audio IC

SAA2505H

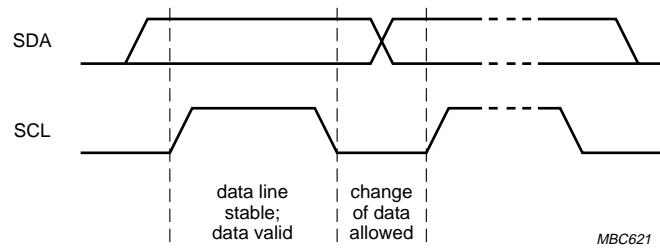


Fig.5 Bit transfer on the I²C-bus.

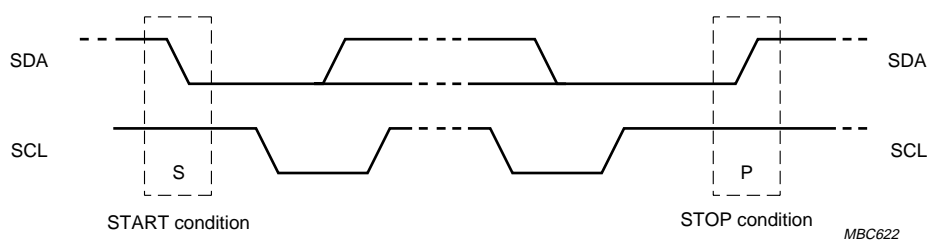


Fig.6 START and STOP conditions.

DUET digital multichannel audio IC

SAA2505H

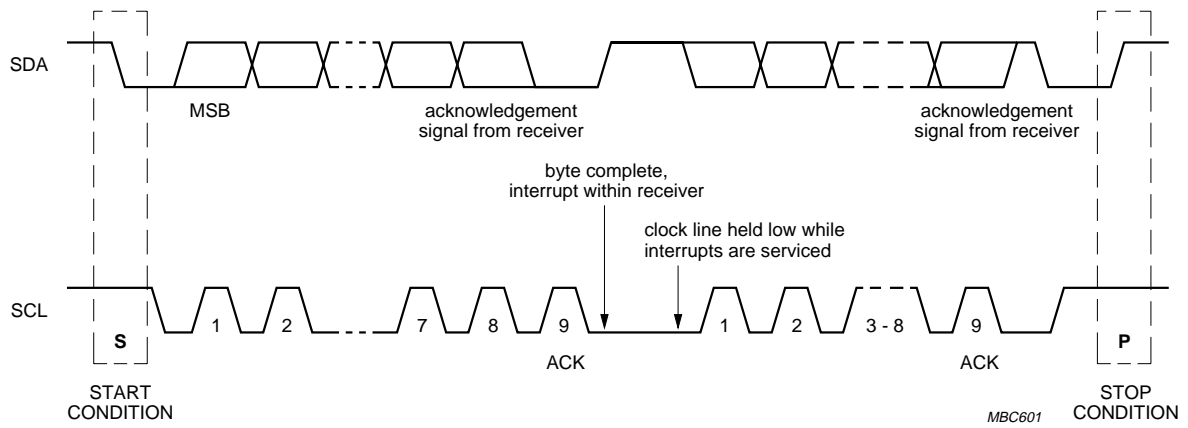


Fig.7 Data transfer on the I²C-bus.

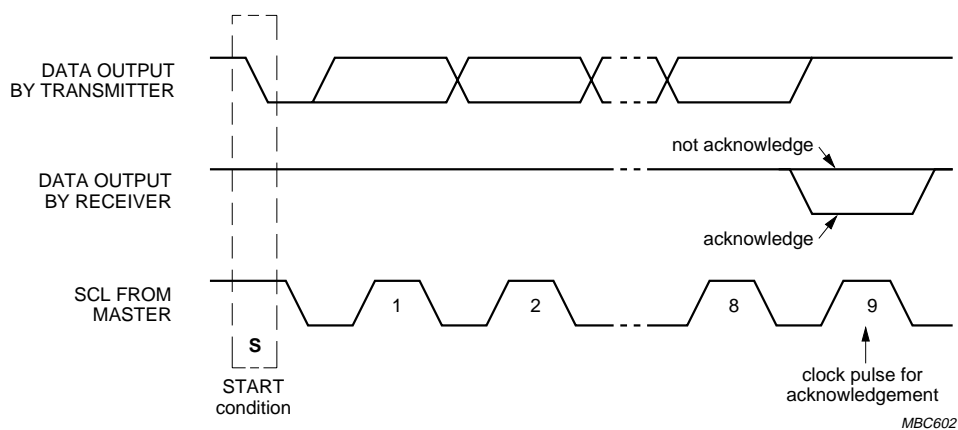


Fig.8 Acknowledge on the I²C-bus.

DUET digital multichannel audio IC

SAA2505H

I²C-bus format

ADDRESSING

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

SLAVE ADDRESS SELECTION (PIN 62)

The SAA2505H acts as slave receiver or a slave transmitter. Therefore the clock signal (SCL) is only an input signal. The data signal (SDA) is a bidirectional line. The SAA2505H slave addresses are shown in Table 4.

Table 4 I²C-bus address

I ² C-BUS LEVEL	I ² C-BUS ADDRESS
1	59H
0	58H

The subaddress bit A0 corresponds to the hardware address at pin 52 which allows the device to have 2 different addresses. This allows control of two DUET ICs via the same I²C-bus.

WRITE AND READ CYCLES

The I²C-bus configuration for a write cycle is shown in Table 5. The write cycle is used to write the bytes to memory and control registers.

The I²C-bus configuration for a read cycle is shown in Table 6. The read cycle is used to read bytes from memory and control registers.

Table 5 I²C-bus write sequence

I ² C-BUS MASTER	SAA2505H
START	–
I ² C-bus address of SAA2505H	–
Write	–
–	acknowledge
Address high part	–
–	acknowledge
Address low part	–
–	acknowledge
Data high part	–
–	acknowledge
Data medium part	–
–	acknowledge
Data low part	–
–	acknowledge
Data high part	–
–	acknowledge
Data medium part	–
–	acknowledge
Data low part	–
–	acknowledge
Continued exchanges	
STOP Condition	–

DUET digital multichannel audio IC

SAA2505H

Table 6 I²C-bus read sequence

I ² C-BUS MASTER	SAA2505H
START	–
I ² C-bus address of SAA2505H	–
Write	–
–	acknowledge
Address high part	–
–	acknowledge
Address low part	–
–	acknowledge
START	–
I ² C-bus address of SAA2505H	–
Read	–
–	acknowledge
–	data high part
–	acknowledge
–	data medium part
–	acknowledge
–	data low part
–	acknowledge
–	data high part
–	acknowledge
–	data medium part
–	acknowledge
–	data low part
–	acknowledge
Continued Exchanges	
STOP Condition	–

All RAM and peripheral registers are mapped into a common 16-bit address range. The data words are all MSB padded to 24-bit, however, the on-chip RAM is 20-bit and therefore the 4 MSBs are padded with zeros.

Table 7 SAA2505H I²C-bus address ranges

START	STOP	MEMORY BLOCK
\$0	\$1FFF	DSP1 X memory
\$2000	\$3FFF	DSP1 Y memory
\$4000	\$5FFF	DSP2 X memory
\$6000	\$7FFF	DSP2 Y memory
\$8000	\$9FFF	control registers

Power supply connections and EMC

The digital part of the chip has in total 13 positive supply line connections and 13 ground connections. To minimise radiation the device should be put on a double layer PCB with, on one side, a large ground plane. The ground supply lines should have a short connection to this ground plane. The supply line connections should have minimum inter-pin PCB track impedances. A low reactance (Q) ferrite bead/capacitor network in the positive supply line can be used as a high frequency filter. Special attention should be paid to the analog supply lines (V_{DDA} and V_{SSA}).

Boundary scan test interface

The SAA2505H has a 5 pin boundary scan test interface which implements the three required commands of the IEEE1149; BYPASS, SAMPLE and EXTEST.

The boundary scan test interface uses the following pins TDI (pin 47), TMS (pin 48), TCK (pin 49), $\overline{\text{TRST}}$ (pin 50) and TDO (pin 51). Naming and use of the pins is as per IEEE recommendations.

Though $\overline{\text{TRST}}$, TMS and TDI have internal pull-up resistors there should also be system level pull-up resistors.

DUET digital multichannel audio IC

SAA2505H

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		-0.3	+3.3	V
ΔV_{DDD}	voltage difference between two supply voltage pins		-	330	mV
I_{IK}	DC input clamp diode current	$V_I < -0.3\text{ V}$ or $V_I > V_{DDD} + 0.3\text{ V}$	-	± 10	mA
I_{OK}	DC output clamp diode current	output type 4 mA; $V_O < -0.3\text{ V}$ or $V_O > V_{DDD} + 0.3\text{ V}$	-	± 10	mA
I_O	DC output source or sink current	output type 4 mA; $-0.3\text{ V} < V_O < V_{DDD} + 0.3\text{ V}$	-	± 10	mA
I_{DDD} I_{SSD}	DC current per supply pin (V_{DDD} or V_{SSD})		-	± 500	mA
T_{amb}	operating ambient temperature		0	70	°C
T_{stg}	storage temperature range		-55	+125	°C
LTCH	latch-up protection	CIC specification/test method	100	-	mA
V_{ESD}	electrostatic discharge sensitivity for all pins	note 1	-2000	+2000	V
		note 2	-300	+300	V

Notes

- Human body model: equivalent to discharging a 100 pF capacitor through a 1500 Ω resistor.
- Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air	45	K/W

CHARACTERISTICS

Digital I/O at $T_{amb} = 0$ to 70 °C; $V_{DDD} = 3.0$ to 3.6 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3	3.3	3.6	V
V_{DDA}	analog supply voltage for the crystal oscillator		3	3.3	3.6	V
I_{DDD}	digital supply current	$f_{xtal} = 41\text{ MHz}$; maximum activity of the DSP	-	tbf	tbf	mA
$I_{DD(xtal)}$	supply current for the crystal oscillator	$f_{xtal} = 41\text{ MHz}$; functional mode	-	tbf	tbf	mA
P_{tot}	total power dissipation	$f_{xtal} = 41\text{ MHz}$; maximum activity of the DSP	-	tbf	tbf	W
V_{hys}	schmitt trigger hysteresis	pin type SCHMITCD	0.4	-	0.7	V
V_{IH}	HIGH-level input voltage	$I_o = -3\text{ mA}$; pin types A, B and C	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{DDD} = 3.0\text{ V}$; $I_o = 3\text{ mA}$; pin types A, B and C	-	-	0.8	V

DUET digital multichannel audio IC

SAA2505H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{OH}	HIGH-level digital output voltage	I _o = -3 mA; pin types A, B and C	2.4	-	-	V
V _{OL}	LOW-level digital output voltage	V _{DDD} = 3.0 V; I _o = 3 mA; pin types A, B and C	-	-	0.4	V
V _{OL(I2C)}	LOW-level digital output voltage and I ² C-bus data output	I _o = 8 mA; pin type D	-	-	0.4	V
I _{LO(Z)}	output leakage current, 3-state outputs	V _o = 0 or V _{DDD} ; pin types A, B and C	-	-	±5	μA
R _{pu(int)}	internal pull-up resistor to V _{DDDX}	pin type B	-	76	-	kΩ
R _{pd(int)}	internal pull-down resistor to V _{SSDX}	pin type A	-	76	-	kΩ
t _{i(r)}	input rise time	V _{DDD} = 3.6 V	-	tbf	3.6	ns
t _{i(f)}	input fall time	V _{DDD} = 3.6 V	-	tbf	3.6	ns
t _{o(r)}	output rise time	pin types E, F and G; V _{DDD} = 3.3 V; T _{amb} = 25 °C; process = 0 σ; C _L = 20 pF	-	-	3.0	ns
t _{o(f)}	output fall time	pin types E, F and G; V _{DDD} = 3.3 V; T _{amb} = 25 °C; process = 0 σ; C _L = 20 pF	-	-	3.5	ns
Oscillator input/output						
f _{xtal}	crystal frequency		40	40.5	-	MHz
V _{xtal}	voltage across the crystal		3.0	3.3	3.6	V
g _m	transconductance	at start-up	10.5	19	32	mS
		in operating range	3.6	-	38	mS
C _{L(CLK)}	capacitive load of clock output		-	500	1000	fF
T _{cy(STRTU)}	number of cycles in start-up time	depends on quality of the external crystal	-	1000	-	cycles

DUET digital multichannel audio IC

SAA2505H

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Serial digital inputs and outputs; (see Fig.9)					
t_r	rise time	$T_{cy} = 50 \text{ ns}$	–	7.5	ns
t_f	fall time	$T_{cy} = 50 \text{ ns}$	–	7.5	ns
T_{cy}	bit clock cycle time		70	–	ns
$t_{BCK(H)}$	bit clock time HIGH	$T_{cy} = 50 \text{ ns}$	17.5	–	ns
$t_{BCK(L)}$	bit clock time LOW	$T_{cy} = 50 \text{ ns}$	17.5	–	ns
$t_{s;DAT}$	data set-up time host	$T_{cy} = 50 \text{ ns}$	320	–	ns
$t_{s;DAT}$	data set-up time I ² S-bus input		10	–	ns
$t_{h;DAT}$	data hold time host	$T_{cy} = 50 \text{ ns}$	50	–	ns
$t_{h;DAT}$	data hold time I ² S-bus input		10	–	ns
$t_{s;WS}$	word select set-up time I ² S-bus input	$T_{cy} = 50 \text{ ns}$	100	–	ns
$t_{h;WS}$	word select hold time I ² S-bus input	$T_{cy} = 50 \text{ ns}$	100	–	ns
$t_{d;DAT}$	data delay time host		–	20	ns
$t_{d;WS}$	word select delay time host		–	15	ns
I²C-bus timing; (see Fig.10)					
f_{SCL}	SCL clock frequency		0	400	kHz
t_{BUF}	bus free between a STOP and START condition		1.3	–	μs
$t_{HD;STA}$	hold time (repeated) start condition; after this period the first clock pulse is generated		0.6	–	μs
t_{LOW}	LOW period of the SCL clock		1.3	–	μs
t_{HIGH}	HIGH period of the SCL clock		0.6	–	μs
$t_{SU;STA}$	set-up time for a repeated start condition		0.6	–	μs
$t_{HD;DAT}$	data hold time		0	0.9	μs
$t_{SU;DAT}$	data set-up time	for standard mode I ² C-bus system $t_{SU;DAT} > 250 \text{ ns}$	100	–	ns
t_r	rise time of both SDA and SCL signals	$f_{SCL} = 400 \text{ kHz}$	$20 + 0.1C_{bus}^{(1)}$	300	ns
		$f_{SCL} = 100 \text{ kHz}$	$20 + 0.1C_{bus}^{(1)}$	1000	ns
t_f	fall time of both SDA and SCL signals		$20 + 0.1C_{bus}^{(1)}$	300	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	μs
$C_{L(bus)}$	capacitive load for each bus line		–	400	pF
t_{SP}	pulse width of spikes which must be suppressed by the input filter	$f_{SCL} = 400 \text{ kHz}$	0	50	ns

Note

- C_{bus} = bus line capacitance in pF.

DUET digital multichannel audio IC

SAA2505H

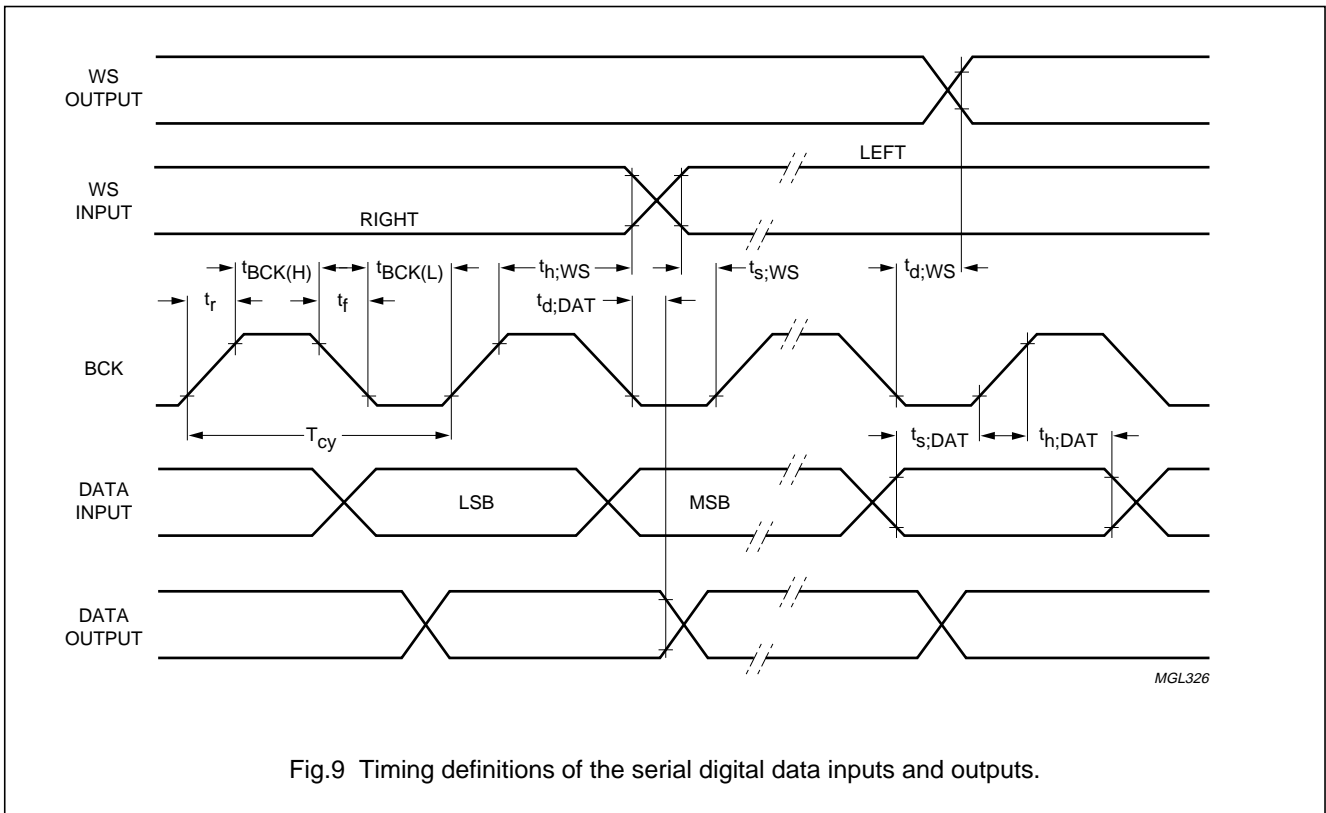
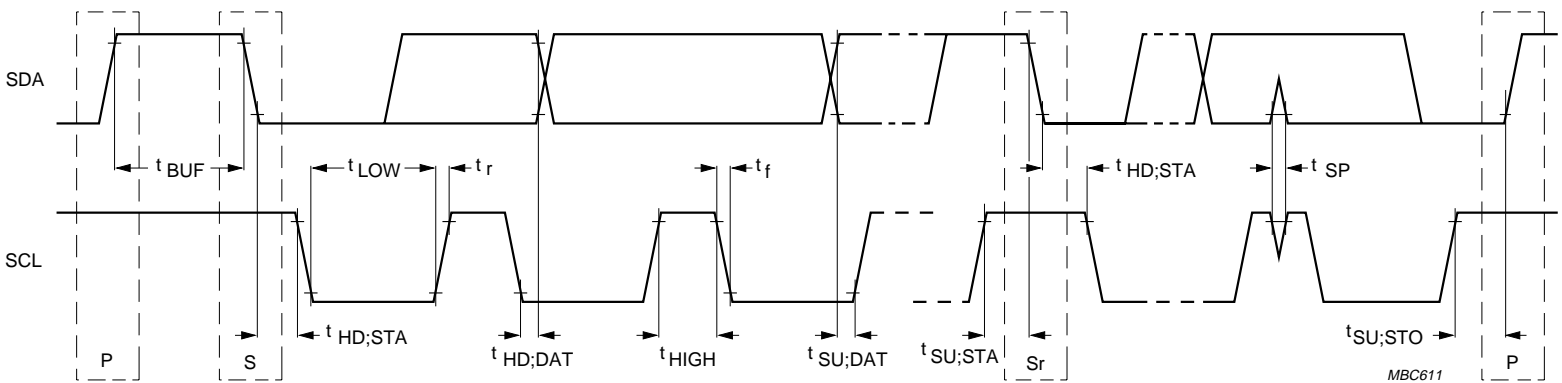


Fig.9 Timing definitions of the serial digital data inputs and outputs.

DUET digital multichannel audio IC

SAA2505H



MBC611

Fig.10 Timing definition of the I²C-bus.

DUET digital multichannel audio IC

SAA2505H

APPLICATION INFORMATION

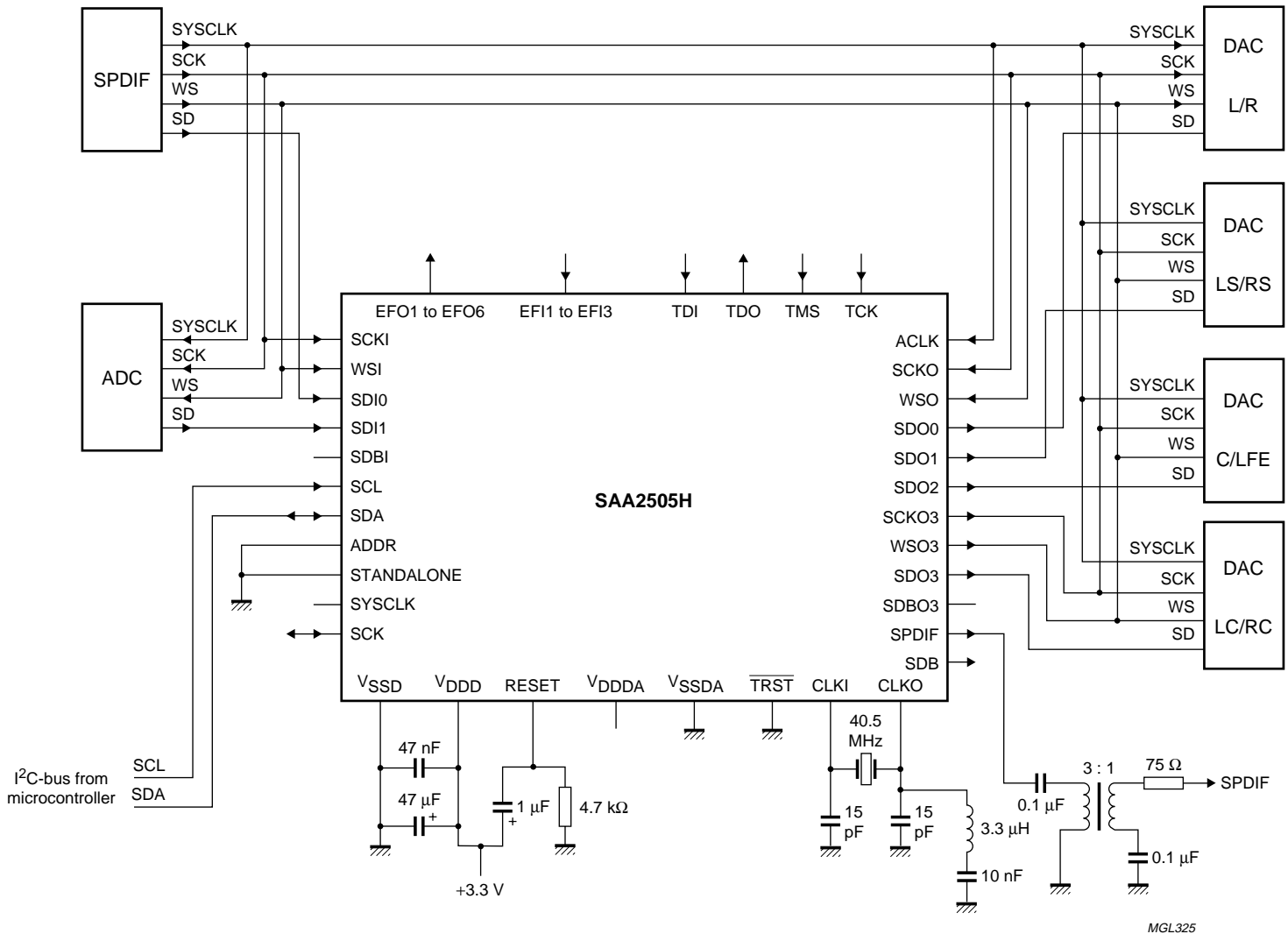


Fig.11 Application diagram for SAA2505H.

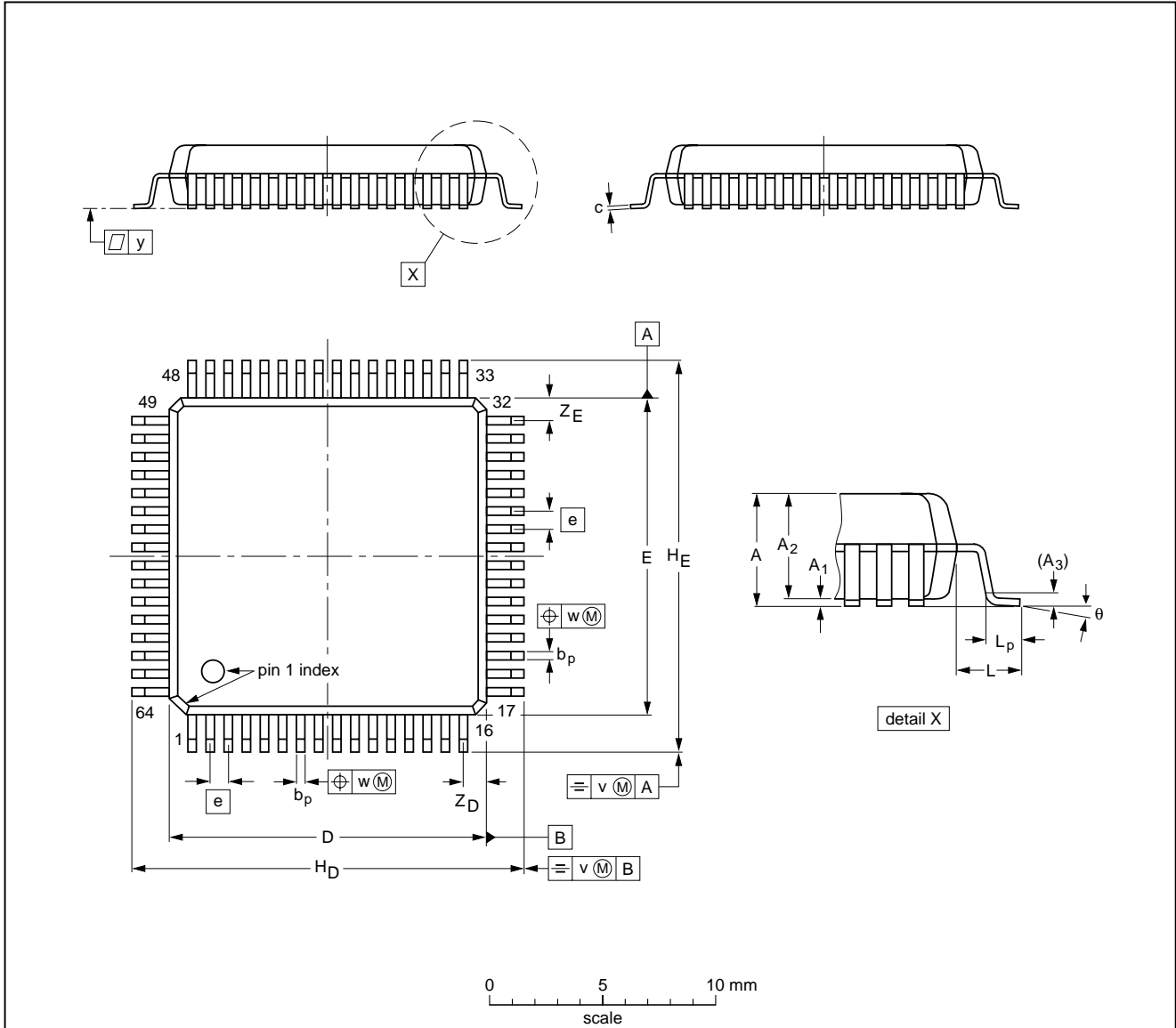
DUET digital multichannel audio IC

SAA2505H

PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm

SOT393-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	3.00	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.60	1.03 0.73	0.16	0.16	0.10	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT393-1	134E07	MS-022				99-12-27 00-01-19

DUET digital multichannel audio IC

SAA2505H

SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our "Quality Reference Handbook" (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

CAUTION

Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

DUET digital multichannel audio IC

SAA2505H

DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

ICs with MPEG-2 functionality — Use of this product in any manner that complies with the MPEG-2 Standard is expressly prohibited without a license under applicable patents in the MPEG-2 patent portfolio, which license is available from MPEG LA, L.L.C., 250 Steele Street, Suite 300, Denver, Colorado 80206.

DUET digital multichannel audio IC

SAA2505H

PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

DUET digital multichannel audio IC

SAA2505H

NOTES

DUET digital multichannel audio IC

SAA2505H

NOTES

DUET digital multichannel audio IC

SAA2505H

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 7 - 9 Rue du Mont Valérien, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4728 6600, Fax. +33 1 4728 6638

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: Philips Hungary Ltd., H-1119 Budapest, Fehervari ut 84/A,
Tel: +36 1 382 1700, Fax: +36 1 382 1800

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors,
Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN,
The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 2001

SCA 72

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

753503/02/pp32

Date of release: 2001 Apr 05

Document order number: 9397 750 08201

Let's make things better.

**Philips
Semiconductors**



PHILIPS